Cascaded Programming Circuits using AT17(A) Configurators with Atmel, Xilinx® and Altera® FPGAs

Atmel AT17A [1] series configurators use a simple serial-access procedure to configure one or more Field Programmable Gate Arrays (FPGAs) or Field Programmable System Level Integrated Circuits (FPSLIC™) devices.

This application note provides circuits showing how to perform In-System Programming (ISP) on two cascaded AT17(A) devices, as well as how to use these devices to configure Atmel, Xilinx and Altera FPGAs.

The A2 input of cascaded configurators must be used as an address pin (set to logic level “0” for one configurator and logic level “1” for the other). Each configurator responds only to messages from the programming interface bearing its unique address.

The A2 pin of the AT17LVXXX and AT17LVXXXA series configurator has internal weak pull-down circuitry. However, the A2 pin of the AT17FXXX an AT17FXXXA series configurator has internal weak pull-up resistor. This default setting of the A2 pin requires the appropriate A2 bit level setting in the message of the programming software.

To enter programming mode, the $\overline{\text{SER\_EN}}$ pin has to be set to logic Low. For in-system programming, this is accomplished by connecting the 10-pin ISP connector to the ISP cable. Since pin 10 of the ISP cable is connected to GND, $\overline{\text{SER\_EN}}$ is grounded automatically.

For drop-in/stand-alone programming, the $\overline{\text{SER\_EN}}$ pin is set to logic Low by the programmer.

In configuration mode, the $\overline{\text{SER\_EN}}$ pin has to be set to logic High. For In-system programming, this can be achieved by releasing the ISP cable to allow the external pull-up resistor to pull the $\overline{\text{SER\_EN}}$ pin to V_{CC} (High). For stand-alone and drop-in programming, the $\overline{\text{SER\_EN}}$ pin can be directly connected to V_{CC}.

1. AT17(A) = AT17/AT17A
   AT17 = AT17LV/FXXX
   AT17A = AT17LV/FXXXA
   AT17NXXX series configurators should not be used in the cascaded circuits of this document.

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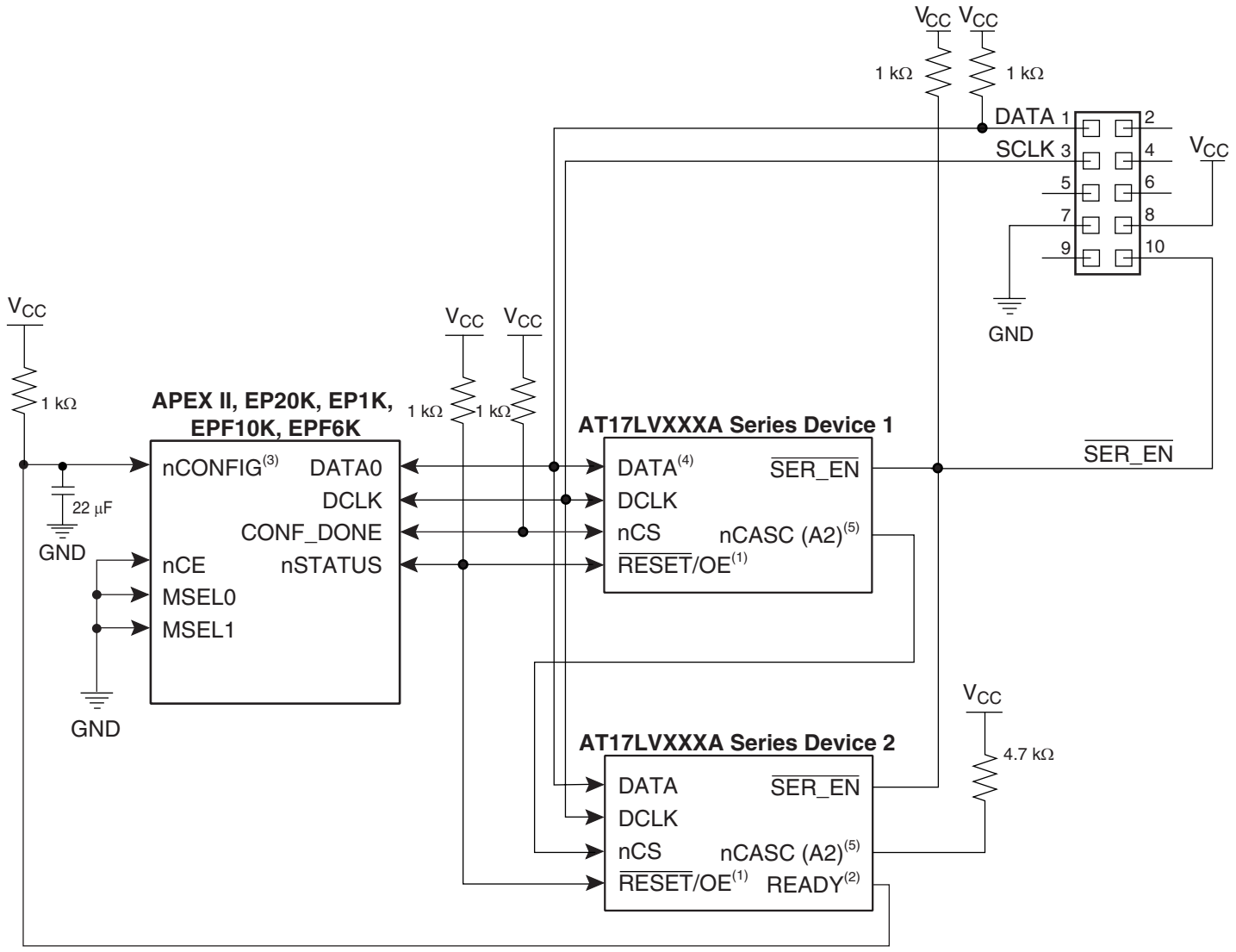
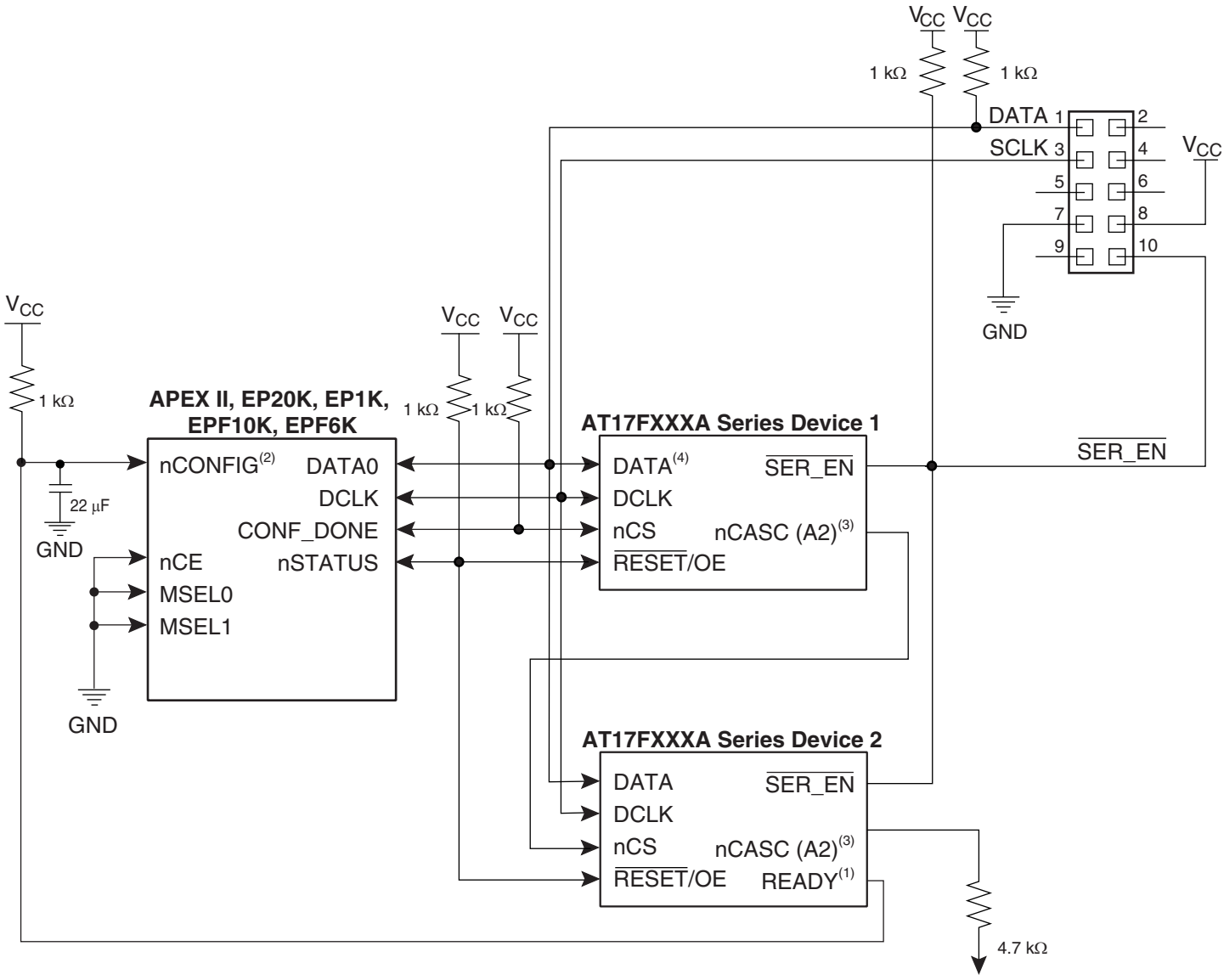
The In-System Programming (ISP) circuit diagrams are shown in Figures 1 through 4. Atmel ATDH2200E or ATDH2225 ISP download cable is recommended to use for the ISP circuit. Refer to the ATDH2200E or ATDH2225 user guides, available on the Atmel web site, for the ISP programming procedure.

Figure 1. ISP of AT17LVXXXA Series Devices for Altera FPGA Applications, Internal Oscillator and Cascaded Arrangement



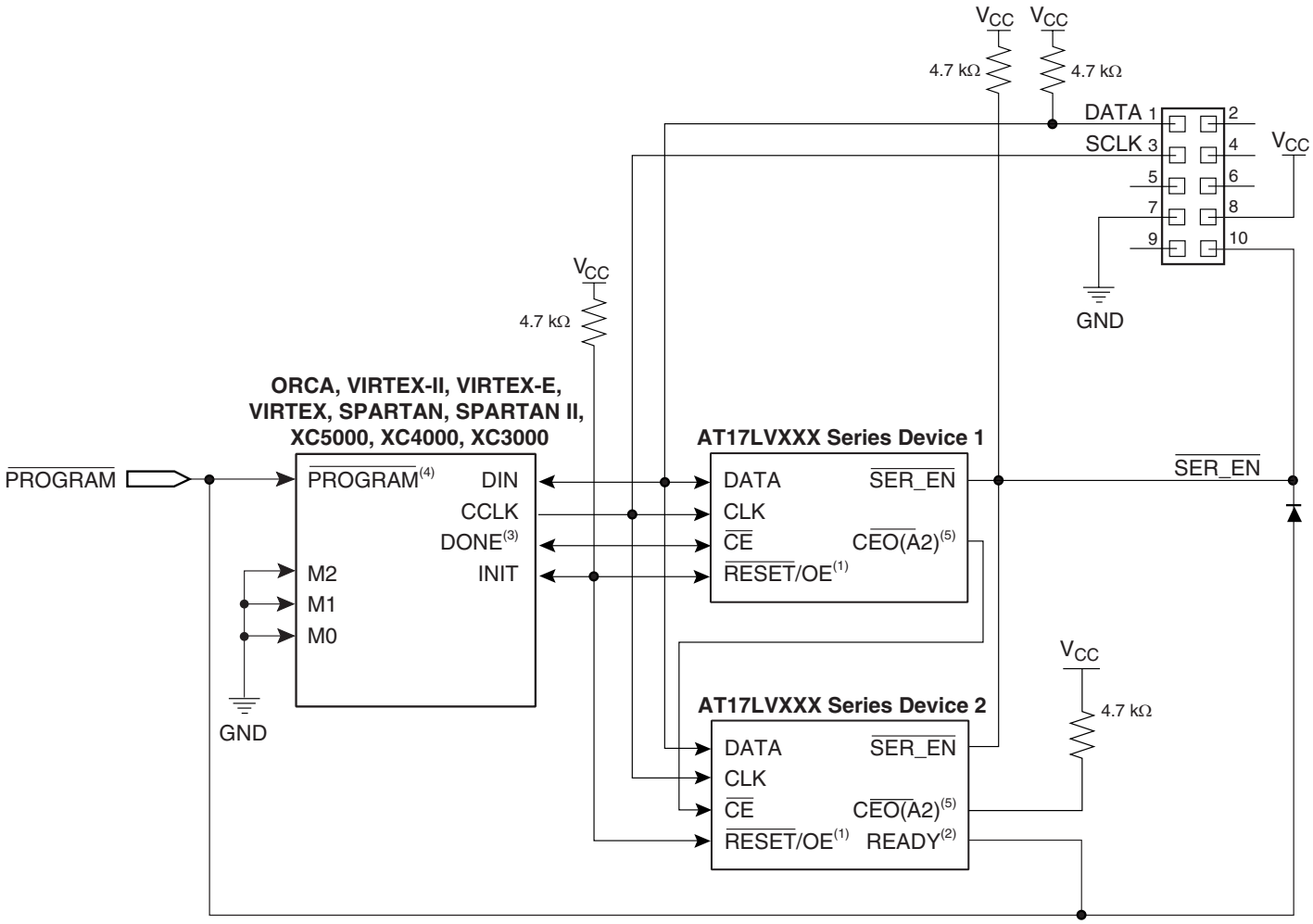
Notes:
1. Reset polarity level of the configurator must be set to active Low ($\overline{\text{RESET}}$/OE) by ISP programmer.
2. Use of the READY pin is optional.
3. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable. nCONFIG can instead be connected to an active Low system reset signal. The capacitor is only recommended if slow or fast power up ramp rate of the power supply is used.
4. The internal oscillator of the second cascaded configurator must be disabled by the programmer.
5. The A2 bit level setting in the Configurator Programming System (CPS) software must be set to low for ISP access to Series Device 1, and set to high for Series Device 2.

Figure 2. ISP of AT17FXXXA Series Devices for Altera FPGA Applications, Internal Oscillator and Cascaded Arrangement



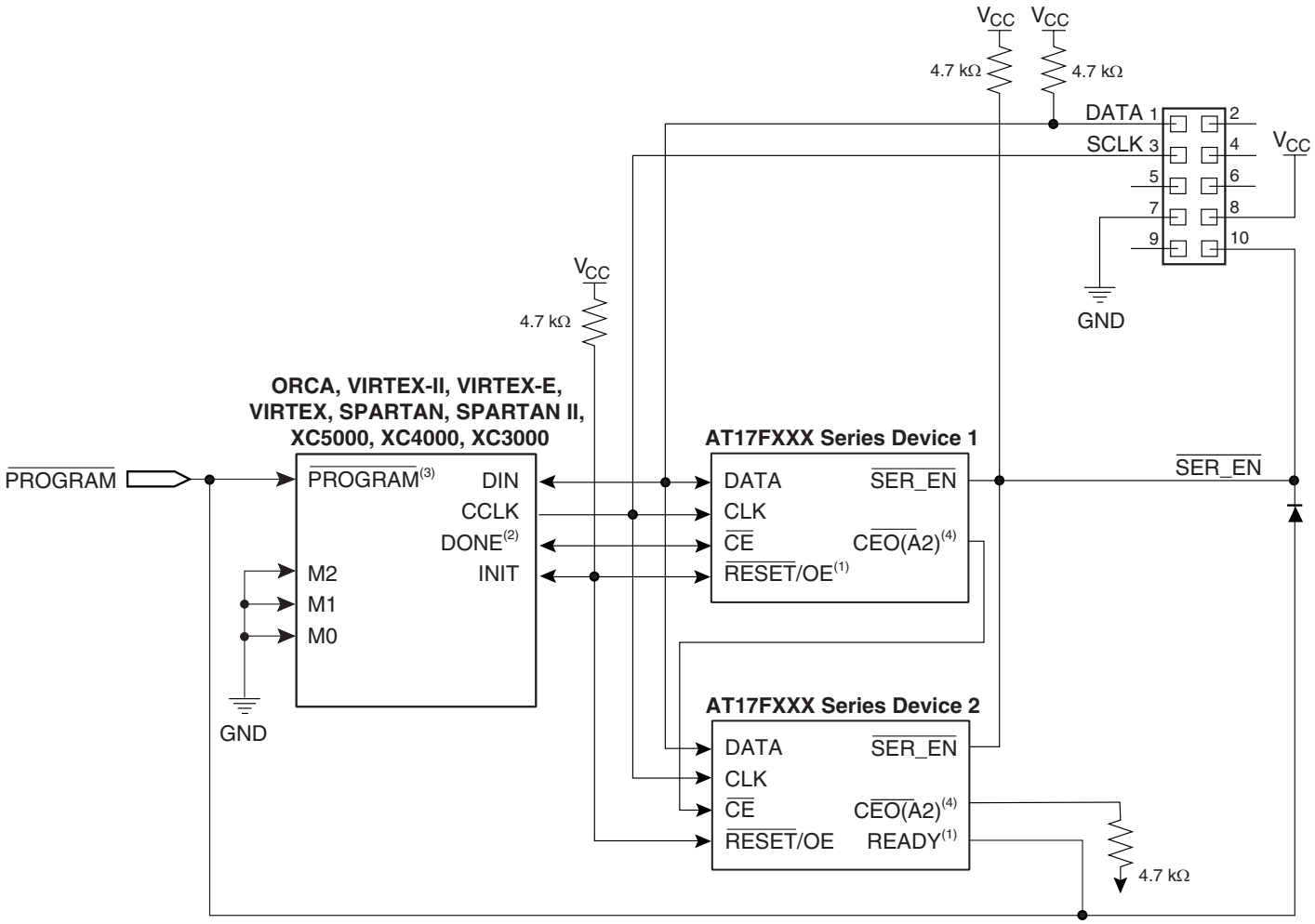
Note:
1. Use of the READY pin is optional.
2. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable. nCONFIG can instead be connected to an active Low system reset signal. The capacitor is only recommended if slow or fast power up ramp rate of the power supply is used.
3. The A2 bit level setting in the Configurator Programming System (CPS) software must be set to high for ISP access to Series Device 1, and set to low for Series Device 2.

Figure 3. ISP of AT17LVXXX Series for Xilinx/Lattice® FPGA Applications, Cascaded Arrangement



Notes:
1. Reset polarity level of the configurator must be set to active Low ($\overline{\text{RESET}}$/OE) by ISP programmer.
2. Use of the READY pin is optional.
3. A 330Ω external pull-up resistor on the DONE pin is required for Virtex® and Virtex-II FPGAs. Xilinx FPGAs can use $\overline{\text{LDC}}$ instead of the DONE pin.
4. Xilinx FPGAs can use $\overline{\text{RESET}}$ instead of the $\overline{\text{PROGRAM}}$ pin. ORCA® FPGAs can use $\overline{\text{PRGM}}$ instead of the $\overline{\text{PROGRAM}}$ pin.
5. The A2 bit level setting in the Configurator Programming System (CPS) software must be set to low for ISP access to Series Device 1, and set to high for Series Device 2.

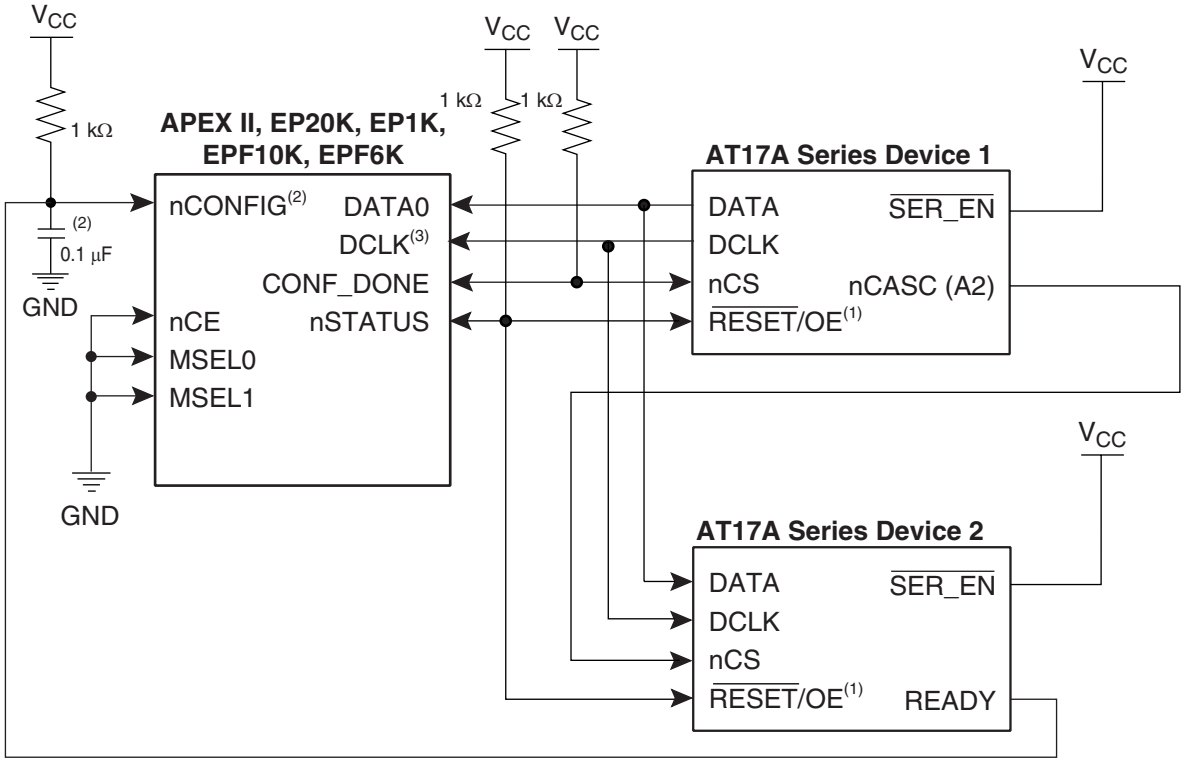
Figure 4. ISP of AT17FXXX Series for Xilinx/Lattice® FPGA Applications, Cascaded Arrangement



Notes:
1. Use of the READY pin is optional.
2. A 330Ω external pull-up resistor on the DONE pin is required for Virtex® and Virtex-II FPGAs. Xilinx FPGAs can use $\overline{\text{LDC}}$ instead of the DONE pin.
3. Xilinx FPGAs can use $\overline{\text{RESET}}$ instead of the $\overline{\text{PROGRAM}}$ pin. ORCA® FPGAs can use $\overline{\text{PRGM}}$ instead of the $\overline{\text{PROGRAM}}$ pin.
4. The A2 bit level setting in the Configurator Programming System (CPS) software must be set to high for ISP access to Series Device 1, and set to low for Series Device 2.

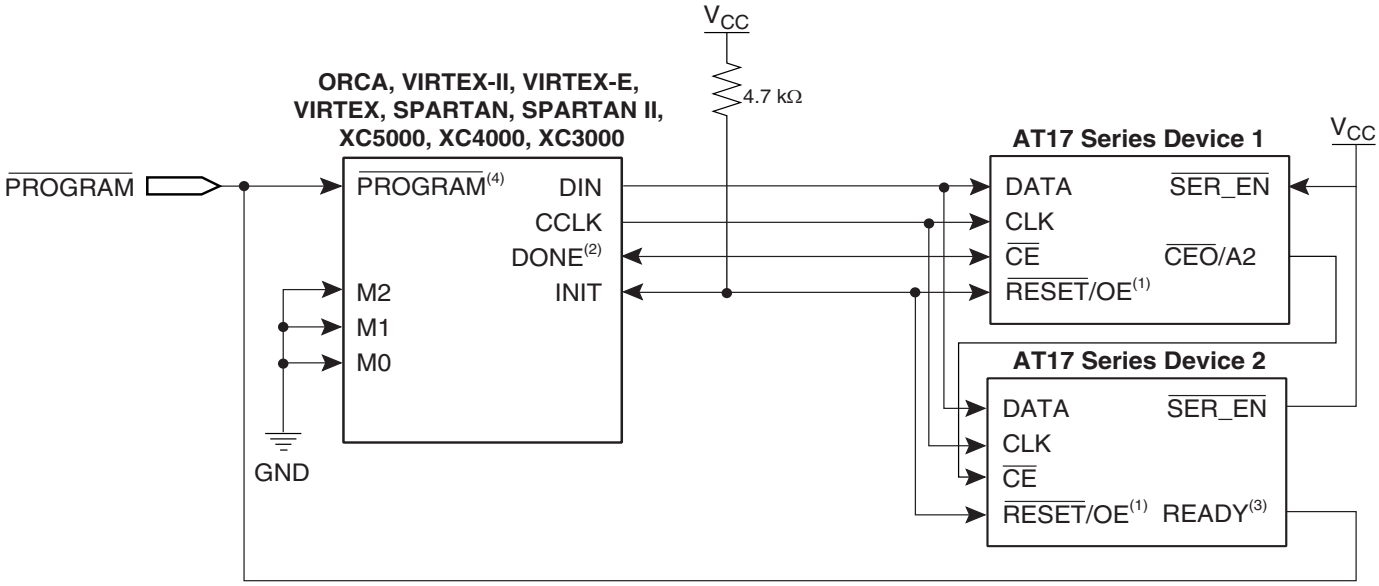
The Drop-in/stand-alone programming circuit diagrams are displayed in Figure 5 and Figure 6. Atmel ATDH2200E programming kit and many other third-party programmers can be used to program the configuration bitstream to the EEPROMs, before the parts are placed into the drop-in/stand-alone programming circuits.

Figure 5. Drop-In Replacement of AT17A Devices for Altera FPGAs, Internal Oscillator and Cascaded Arrangement



Notes:
1. Reset polarity level of the configurator must be set to active Low ($\overline{\text{RESET}}$/OE) by programmer if AT17LVXXXA series configurators are used.
2. RC filter recommended for input to nCONFIG to delay configuration until Vcc is stable. nCONFIG can instead be connected to an active Low system reset signal. The capacitor is only recommended if slow or fast power up ramp rate of the power supply is used.
3. If AT17LVXXXA series configurators are used, the internal oscillator of the DCLK pin of the second configurator must be disabled to avoid clock contention.

Figure 6. Drop-In Replacement of AT17 Series Devices for Xilinx and Lattice Applications, Cascaded Arrangement



Notes:
1. Reset polarity level of the configurator must be set to active Low ($\overline{\text{RESET}}$/OE) by programmer if AT17LVXXX series configurators are used.
2. A 330Ω external pull-up resistor on the DONE pin is required for Virtex and Virtex-II FPGAs. Xilinx FPGAs can use $\overline{\text{LDC}}$ instead of the DONE pin.
3. Use of the READY pin is optional.
4. Xilinx FPGAs can use $\overline{\text{RESET}}$ instead of the $\overline{\text{PROGRAM}}$ pin. ORCA FPGAs can use $\overline{\text{PRGM}}$ instead of the $\overline{\text{PROGRAM}}$ pin.

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